

**1 D4 - TEKKOM B**



**POST TEST**

**COMPARATOR 2 BIT**



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**POST TEST**

**COMPARATOR 2 BIT**

1. TUJUAN
2. Mahasiswa dapat mendisain rangkaian dari Comparator 2bit.

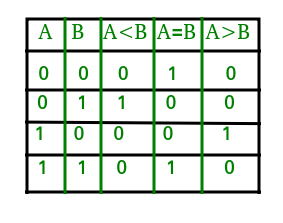
1. TEORI

Fungsi dasar dari komparator adalah untuk membandingkan magnitudo relatif dua kuantitas. Komparator mempunyai tiga output :

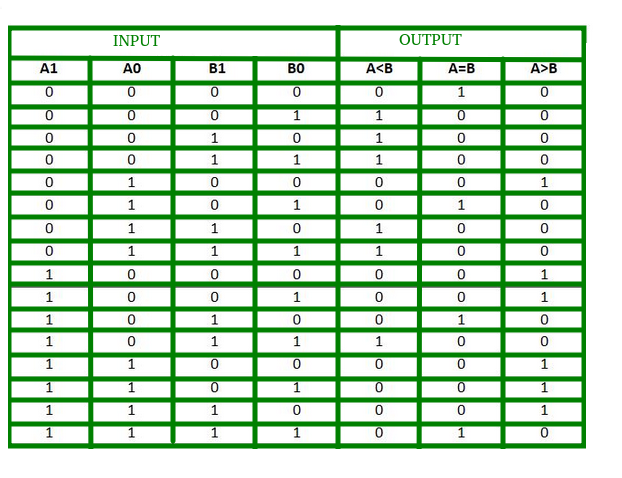
* A=B (A sama dengan B)
* A>B (A lebih besar dari B)
* A<B (A kurang dari B)

Hanya satu dari tiga output dapat TINGGI. Output tinggi memberitahu bahwa apakah bit digital lebih kecil, lebih besar, atau sama dari input binary.

Tabel Kebenaran dari Comparator 1 digit.



Tabel Kebenaran dari Comparator 2 digit.



1. ALAT DAN BAHAN
2. Software ISE Design Suite Xilinx
3. LANGKAH PERCOBAAN
4. Comparator Statement pengkondisian
5. Code VHDL Statement pengkondisian

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity code\_comp\_cond is

port (

a : in std\_logic\_vector (1 downto 0);

b : in std\_logic\_vector (1 downto 0);

x, y, z : out std\_logic

);

end code\_comp\_cond;

architecture Behavioral of code\_comp\_cond is

begin

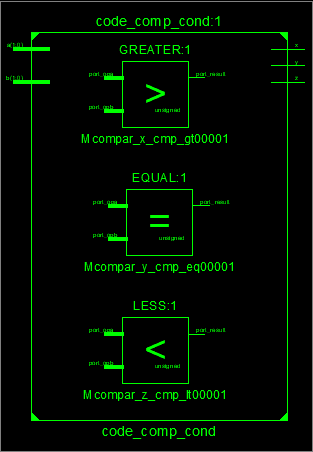
x <= '1' when (a > b) else '0';

y <= '1' when (a = b) else '0';

z <= '1' when (a < b) else '0';

end Behavioral;

1. RTL Schematic Statement Pengkondisian



1. TestBench Statement pengkondisian

LIBRARY ieee;

USE ieee.std\_logic\_1164.ALL;

ENTITY tb\_comp\_cond IS

END tb\_comp\_cond;

ARCHITECTURE behavior OF tb\_comp\_cond IS

-- Component Declaration for the Unit Under Test (UUT)

COMPONENT code\_comp\_cond

PORT(

a : IN std\_logic\_vector(1 downto 0);

b : IN std\_logic\_vector(1 downto 0);

x : OUT std\_logic;

y : OUT std\_logic;

z : OUT std\_logic

);

END COMPONENT;

--Inputs

signal a : std\_logic\_vector(1 downto 0) := (others => '0');

signal b : std\_logic\_vector(1 downto 0) := (others => '0');

--Outputs

signal x : std\_logic;

signal y : std\_logic;

signal z : std\_logic;

-- No clocks detected in port list. Replace <clock> below with

-- appropriate port name

BEGIN

-- Instantiate the Unit Under Test (UUT)

uut: code\_comp\_cond PORT MAP (

a => a,

b => b,

x => x,

y => y,

z => z

);

stim\_proc: process

begin

a <= "00";

b <= "00";

wait for 50 ns;

b <= "01";

wait for 50 ns;

b <= "10";

wait for 50 ns;

b <= "11";

wait for 50 ns;

a <= "01";

b <= "00";

wait for 50 ns;

b <= "01";

wait for 50 ns;

b <= "10";

wait for 50 ns;

b <= "11";

wait for 50 ns;

a <= "10";

b <= "00";

wait for 50 ns;

b <= "01";

wait for 50 ns;

b <= "10";

wait for 50 ns;

b <= "11";

wait for 50 ns;

a <= "11";

b <= "00";

wait for 50 ns;

b <= "01";

wait for 50 ns;

b <= "10";

wait for 50 ns;

b <= "11";

wait for 50 ns;

wait;

end process;

END;

wait for 50 ns;

b <= "01";

wait for 50 ns;

b <= "10";

wait for 50 ns;

b <= "11";

wait for 50 ns;

a <= "10";

b <= "00";

wait for 50 ns;

b <= "01";

wait for 50 ns;

b <= "10";

wait for 50 ns;

b <= "11";

wait for 50 ns;

a <= "11";

b <= "00";

wait for 50 ns;

b <= "01";

wait for 50 ns;

b <= "10";

wait for 50 ns;

b <= "11";

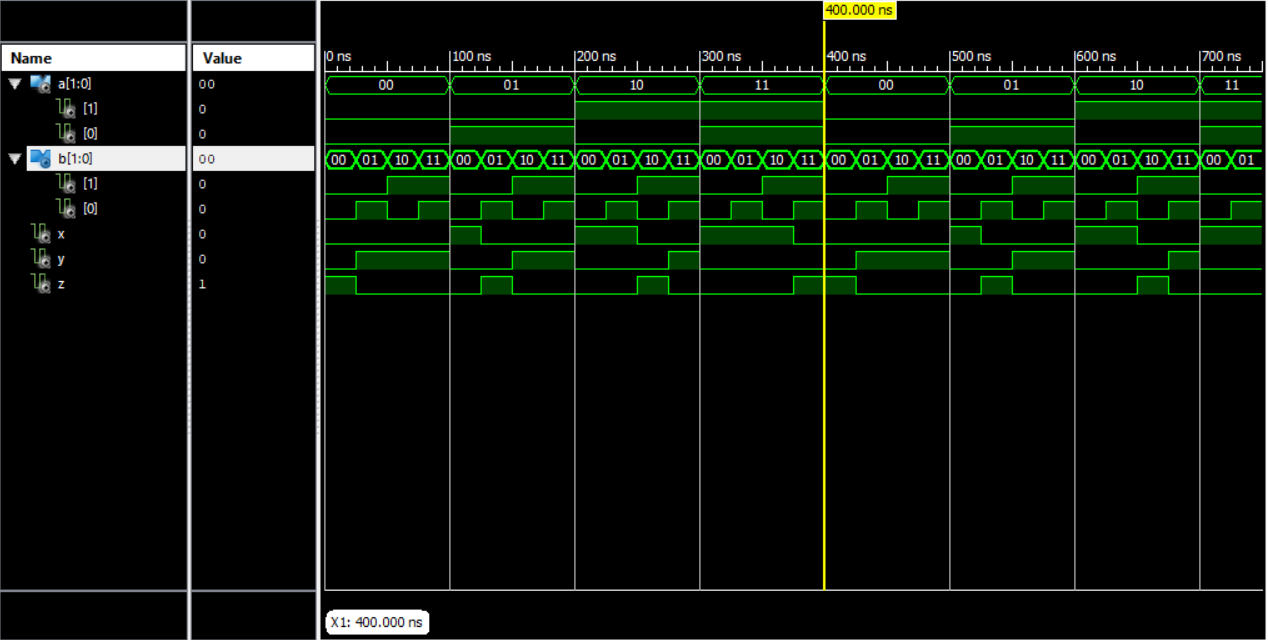
wait for 50 ns;

wait;

end process;

END;

1. Timing Diagram Statement pengkondisian



1. Comparator Seleksi Sinyal
2. Code VHDL Seleksi Sinyal

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity code\_comp\_sinyal is

port (

a, b : in std\_logic\_vector (1 downto 0);

x, y, z : out std\_logic

);

end code\_comp\_sinyal;

architecture Behavioral of code\_comp\_sinyal is

signal s : std\_logic\_vector (3 downto 0);

begin

s <= a & b;

with s select

x <= '1' when "0100" | "1000" | "1001" | "1100" | "1101" | "1110",

'0' when others;

with s select

y <= '1' when "0000" | "0101" | "1010" | "1111",

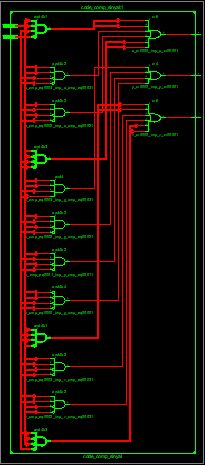
'0' when others;

with s select

z <= '1' when "0001" | "0010" | "0011" | "0110" | "0111" | "1011",

'0' when others;

end Behavioral;

1. RTL Seleksi Sinyal
2. TestBench Seleksi Sinyal

LIBRARY ieee;

USE ieee.std\_logic\_1164.ALL;

ENTITY tb\_comp\_sinyal IS

END tb\_comp\_sinyal;

ARCHITECTURE behavior OF tb\_comp\_sinyal IS

-- Component Declaration for the Unit Under Test (UUT)

COMPONENT code\_comp\_sinyal

PORT(

a : IN std\_logic\_vector(1 downto 0);

b : IN std\_logic\_vector(1 downto 0);

x : OUT std\_logic;

y : OUT std\_logic;

z : OUT std\_logic

);

END COMPONENT;

--Inputs

signal a : std\_logic\_vector(1 downto 0) := (others => '0');

signal b : std\_logic\_vector(1 downto 0) := (others => '0');

--Outputs

signal x : std\_logic;

signal y : std\_logic;

signal z : std\_logic;

-- No clocks detected in port list. Replace <clock> below with

-- appropriate port name

BEGIN

-- Instantiate the Unit Under Test (UUT)

uut: code\_comp\_sinyal PORT MAP (

a => a,

b => b,

x => x,

y => y,

z => z

);

-- Stimulus process

stim\_proc: process

begin

a <= "00";

b <= "00";

wait for 50 ns;

b <= "01";

wait for 50 ns;

b <= "10";

wait for 50 ns;

b <= "11";

wait for 50 ns;

a <= "01";

b <= "00";

wait for 50 ns;

b <= "01";

wait for 50 ns;

b <= "10";

wait for 50 ns;

b <= "11";

wait for 50 ns;

a <= "10";

b <= "00";

wait for 50 ns;

b <= "01";

wait for 50 ns;

b <= "10";

wait for 50 ns;

b <= "11";

wait for 50 ns;

a <= "11";

b <= "00";

wait for 50 ns;

b <= "01";

wait for 50 ns;

b <= "10";

wait for 50 ns;

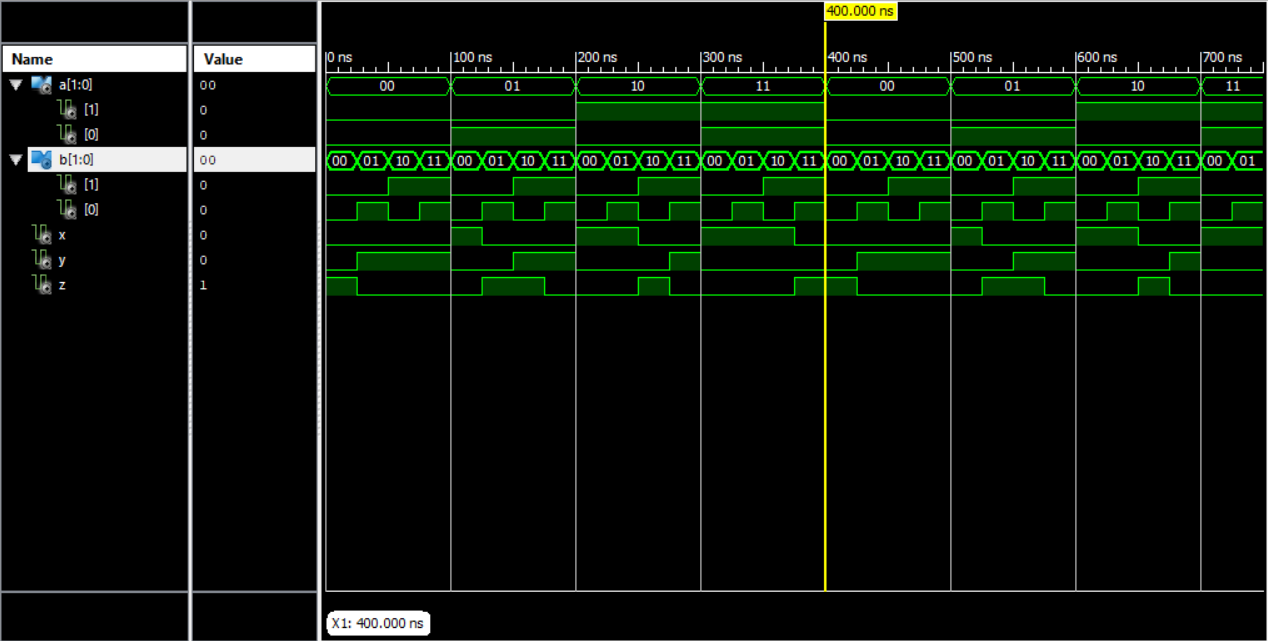
b <= "11";

wait for 50 ns;

wait;

end process;

END;

1. Timing Diagram Seleksi Sinyal
2. Comparator IF statement
3. Code VHDL IF statement

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity comp\_if is

port (

a, b :in std\_logic\_vector (1 downto 0);

x, y, z : out std\_logic

);

end comp\_if;

architecture Behavioral of comp\_if is

begin

process (a, b)

begin

if (a > b) then x <= '1';

else x <= '0';

end if;

if (a = b) then y <= '1';

else y <= '0';

end if;

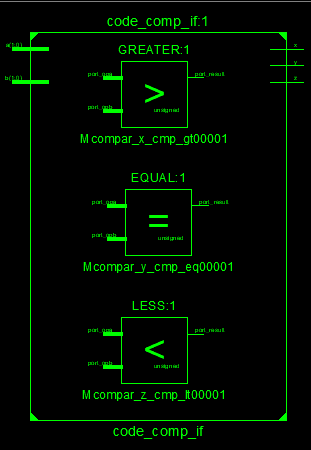
if (a < b) then z <= '1';

else z <= '0';

end if;

end process;

end Behavioral;

1. RTL IF statement
2. TestBench IF statement

LIBRARY ieee;

USE ieee.std\_logic\_1164.ALL;

ENTITY tb\_comp\_if IS

END tb\_comp\_if;

ARCHITECTURE behavior OF tb\_comp\_if IS

-- Component Declaration for the Unit Under Test (UUT)

COMPONENT code\_comp\_if

PORT(

a : IN std\_logic\_vector(1 downto 0);

b : IN std\_logic\_vector(1 downto 0);

x : OUT std\_logic;

y : OUT std\_logic;

z : OUT std\_logic

);

END COMPONENT;

--Inputs

signal a : std\_logic\_vector(1 downto 0) := (others => '0');

signal b : std\_logic\_vector(1 downto 0) := (others => '0');

--Outputs

signal x : std\_logic;

signal y : std\_logic;

signal z : std\_logic;

-- No clocks detected in port list. Replace <clock> below with

-- appropriate port name

BEGIN

A1\_proc: process

begin

wait for 200 ns;

A(1) <= not A(1);

end process;

A0\_proc: process

begin

wait for 100 ns;

A(0) <= not A(0);

end process;

B1\_proc: process

begin

wait for 50 ns;

B(1) <= not B(1);

end process;

B0\_proc: process

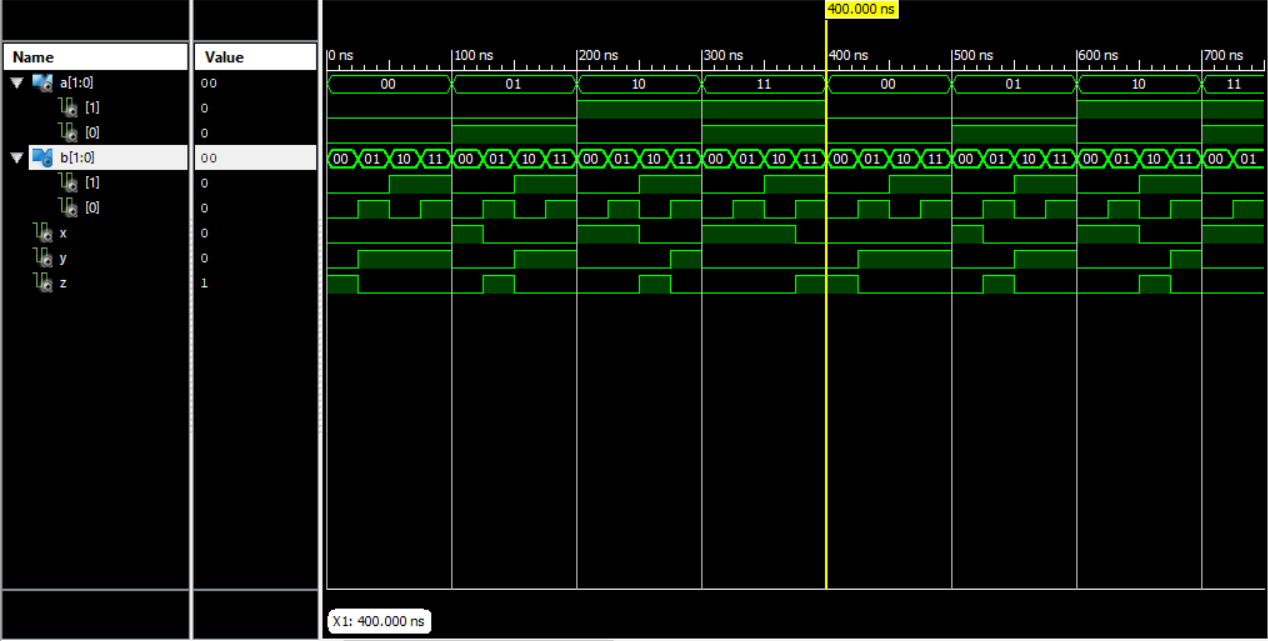
begin

wait for 25 ns;

B(0) <= not B(0);

end process;

END;

1. Timing Diagram IF statement
2. Comparator CASE statement
3. Code VHDL CASE statement

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity code\_comp\_case is

port (

a, b : in std\_logic\_vector (1 downto 0);

x, y, z : out std\_logic

);

end code\_comp\_case;

architecture Behavioral of code\_comp\_case is

signal s : std\_logic\_vector ( 3 downto 0);

begin

s <= a & b;

process (s)

begin

case s is

when "0100" | "1000" | "1001" | "1100" | "1101" | "1110" =>

x <= '1';

when others => x <= '0';

end case;

case s is

when "0000" | "0101" | "1001" | "1010" | "1111" =>

y <= '1';

when others => y <= '0';

end case;

case s is

when "0001" | "0010" | "0011" | "0110" | "0111" | "1011" =>

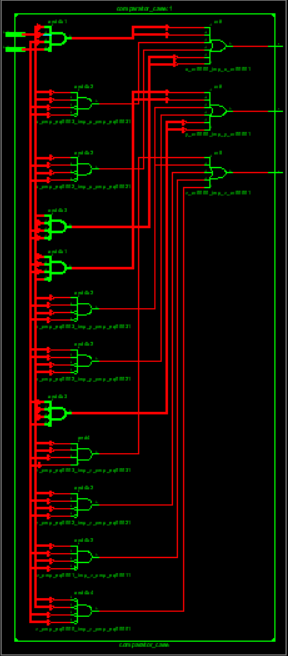
z <= '1';

when others => z <= '0';

end case;

end process;

end Behavioral;

1. RTL CASE statement
2. TestBench CASE statement

LIBRARY ieee;

USE ieee.std\_logic\_1164.ALL;

ENTITY tb\_comp\_case IS

END tb\_comp\_case;

ARCHITECTURE behavior OF tb\_comp\_case IS

-- Component Declaration for the Unit Under Test (UUT)

COMPONENT code\_comp\_case

PORT(

a : IN std\_logic\_vector(1 downto 0);

b : IN std\_logic\_vector(1 downto 0);

x : OUT std\_logic;

y : OUT std\_logic;

z : OUT std\_logic

);

END COMPONENT;

--Inputs

signal a : std\_logic\_vector(1 downto 0) := (others => '0');

signal b : std\_logic\_vector(1 downto 0) := (others => '0');

--Outputs

signal x : std\_logic;

signal y : std\_logic;

signal z : std\_logic;

-- No clocks detected in port list. Replace <clock> below with

-- appropriate port name

BEGIN

-- Instantiate the Unit Under Test (UUT)

uut: code\_comp\_case PORT MAP (

a => a,

b => b,

x => x,

y => y,

z => z

);

-- Stimulus process

stim\_proc: process

begin

a <= "00";

b <= "00";

wait for 50 ns;

b <= "01";

wait for 50 ns;

b <= "10";

wait for 50 ns;

b <= "11";

wait for 50 ns;

a <= "01";

b <= "00";

wait for 50 ns;

b <= "01";

wait for 50 ns;

b <= "10";

wait for 50 ns;

b <= "11";

wait for 50 ns;

a <= "10";

b <= "00";

wait for 50 ns;

b <= "01";

wait for 50 ns;

b <= "10";

wait for 50 ns;

b <= "11";

wait for 50 ns;

a <= "11";

b <= "00";

wait for 50 ns;

b <= "01";

wait for 50 ns;

b <= "10";

wait for 50 ns;

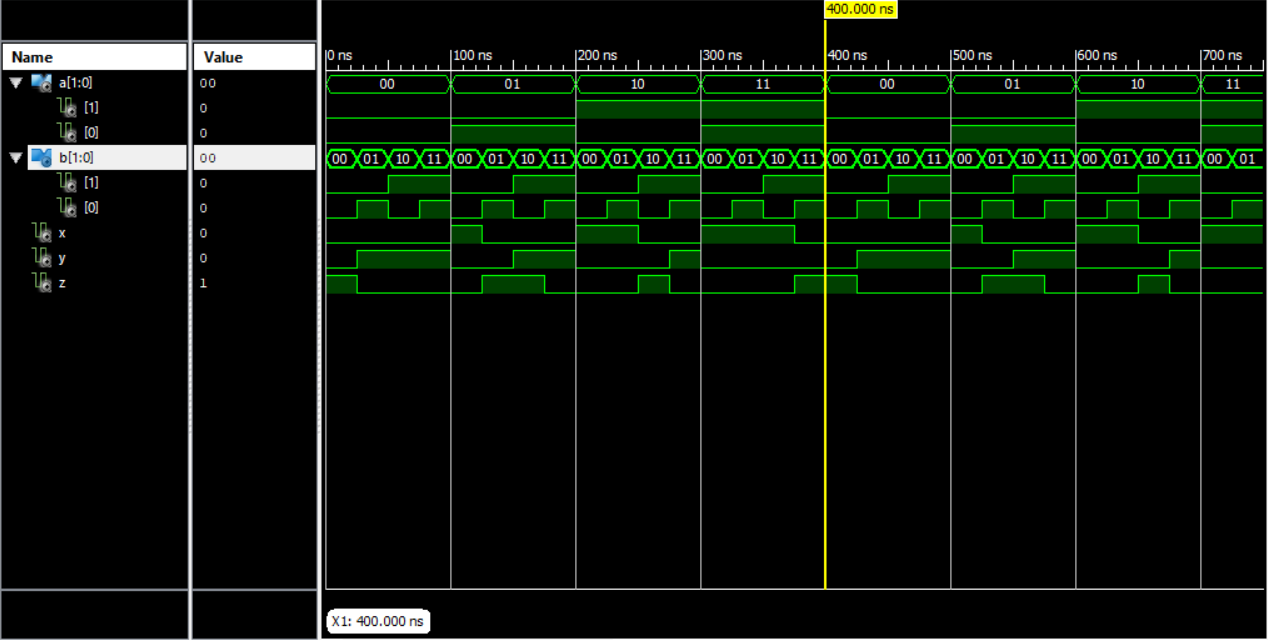
b <= "11";

wait for 50 ns;

wait;

end process;

END;

1. Timing Diagram CASE statement
2. ANALISA

